In the Claims

This listing of claims will replace all prior versions and listings of claims in the application:

1. (Previously Presented) A digital system, comprising:

a memory circuit;

a first requestor circuit with a first memory access node;

a second requestor circuit with a second memory access node;

a scheduling circuit connected to the first memory access node and to the second memory access node and having a request output node, operable to sequentially schedule memory accesses to the memory circuit by the first requestor circuit and by the second request circuit;

a selection circuit connected to the first memory access node and to the scheduling circuit request output node with an output node connected to the memory circuit;

access mode circuitry for indicating at least a first access mode and a second access mode controllably connected to the selection circuit, such that both the first requestor circuit and the second requestor circuit can sequentially access the memory circuit when the access mode circuitry indicates the first access mode and the first requestor circuit has exclusive access to the memory circuit when the access mode circuitry indicates the second access mode; and

a size register for holding a size parameter coupled to the selection circuit, the selection circuit being operable to select a first portion of the memory circuit in response to the size parameter when the access mode circuitry indicates the second access mode, wherein only the first portion of the memory circuit is operable for exclusive access by the first requestor when the access mode circuitry indicates the second access mode.

2. (Original) The digital system of Claim 1, wherein a second portion of the memory circuit not selected in response to the size parameter is operable to be in a low power mode when the access mode circuitry indicates the second access mode.

3. (Original) The digital system according to Claim 1, wherein the selector circuit is operable such that a second portion of the memory circuit not selected in response to the size parameter can be accessed by the second requestor when the access mode circuitry indicates the second access mode.

4. (Original) The digital system according to Claim 1, wherein the size parameter is ignored when the access mode circuitry indicates the first access mode such that the entire memory circuit is operable to be selected for sequential access by the first requestor and the second requestor.

5. (Previously Presented) A digital system comprising:

a memory circuit;

a first requestor circuit with a first memory access node;

a second requestor circuit with a second memory access node;

a scheduling circuit connected to the first memory access node and to the second memory access node and having a request output node, operable to sequentially schedule memory accesses to the memory circuit by the first requestor circuit and by the second request circuit;

a selection circuit connected to the first memory access node and to the scheduling circuit request output node with an output node connected to the memory circuit;

access mode circuitry for indicating at least a first access mode and a second access mode controllably connected to the selection circuit, such that both the first requestor circuit and the second requestor circuit can sequentially access the memory circuit when the access mode circuitry indicates the first access mode and the first requestor circuit has exclusive access to the memory circuit when the access mode circuitry indicates the second access mode;

a size register for holding a size parameter coupled to the selection circuit, the selection circuit being operable to select a first portion of the memory circuit in response to the size parameter when the access mode circuitry indicates the second access mode, wherein only the first portion of the memory circuit is operable for exclusive access by the first requestor when the access mode circuitry indicates the second access mode; and

a clock circuit connected to the second requestor and to the memory circuit, wherein the first portion of the memory circuit operates synchronously with the clock circuit when the access mode circuitry indicates the first access mode and wherein the first portion of the memory circuit operates in an asynchronous manner when the access mode circuitry indicates the second access mode.

6. (Original) The digital system according to Claim 1, wherein the first requester circuit is a host processor and the second requester circuit is direct memory access circuit channel controller.

7. (Canceled)

8. (Original) A method of operating a digital system having a memory circuit that is shared by a plurality of requestor circuits, comprising the steps of:

sharing access to the memory circuit between the plurality of requestor circuits when the digital system is in a first mode of operation;

selecting a first portion of the memory circuit responsive to a size parameter stored in a register, such that a second portion of the memory circuit is not selected; and

limiting access to the first portion of memory circuit to only a first requestor of the plurality of requestors when the digital system is in a second mode of operation.

9. (Original) The method of Claim 8, further comprising the step of sharing access to the second portion of the memory circuit between the plurality of requestor circuits when the digital system is in the second mode of operation.

10. (Original) The method of Claim 8, further comprising the step of placing the second portion of the memory circuit in a low power mode when the digital system is in the second mode of operation.

11. (Previously Presented) The method of Claim 8, wherein the memory has a total size equal to the sum of the first portion and the second portion.

12. (Previously Presented) The method of Claim 11, further comprising the step of storing a different size parameter in the register, such that the step of selecting results in a first

portion having a different size in response to the different size parameter.